REMARKS

Claims 1-34 are pending in the present application. Claims 3, 10, 19, and 30 are currently withdrawn from consideration.

In the office action mailed June 2, 2005 (the "Office Action"), claims 1, 2, 5, 8, 9, 13-15, 17, 18, 21, 24-26, 28, 29, and 32 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,845,409 to Talagala *et al.* (the "Talagala patent"). The Examiner further rejected claims 4, 6, 7, 11, 12, 20, 22, 23, 31, 33, and 34 under 35 U.S.C. 103(a) as being unpatentable over the Talagala patent in view of U.S. Patent Application Publication No. 20030149809 to Jensen *et al.* (the "Jensen application") and rejected claims 16 and 27 under 35 U.S.C. 103(a) as being unpatentable over the Talagala patent in view of U.S. Patent Application Publication No. 20040236885 to Fredriksson *et al.* (the "Fredriksson application").

Information disclosure statements were submitted on July 22, 2003, December 15, 2003, February 25, 2004, April 26, 2004, June 1, 2004, August 13, 2004 and January 21, 2005. Applicant requests the Examiner consider the references cited in each Form PTO-1449 of the Information Disclosure Statements and provide the attorney of record with a signed and initialed copy of each Form PTO-1449.

As previously mentioned, claims 1, 2, 5, 8, 9, 13-15, 17, 18, 21, 24-26, 28, 29, and 32 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Talagala patent.

The Talagala patent is directed to a switch circuit that can create a communication path between a device coupled to a host I/O port, such as a CPU, and one of a plurality of device I/O ports to which different ATA devices can be coupled. *See* col. 7, line 53-col. 8, line 2. The switch is an improvement over the conventional arrangement, as described in the Talagala patent, where an ATA controller is limited to communicating with only two different ATA devices. *See* col. 1, lines 34-41. In contrast, a switch 14 includes several device I/O ports 20 to which a plurality of ATA devices can be coupled. *See* Figure 1 and col. 7, lines 53-59. As with the conventional case, each device I/O port 20 can be coupled to two ATA devices. In one embodiment, two switches 14 are coupled in series so that an even greater number of device I/O ports 20 are available for coupling to ATA devices. *See* Figure 2, col. 8, lines 3-16.

The switch 14 is illustrated in greater detail at col. 8, line 52-col. 9, line 24 and described with reference to Figures 3A and 3B. The switch 14 includes logic 40 coupled between the host I/O port 18 and the device I/O ports 20A-20C. The logic 40 includes a register set 42 that includes addressable registers that are mapped to ATA defined addresses and which are accessed through the host I/O port 18. *See* col. 8, lines 48-61. As shown in Figure 3A, the logic 40 generates power staging signals 44A-44C for selecting and controlling external power supply relays used in providing electrical power to various ATA devices. *See* col. 8, line 62-col. 9, line 2. The logic 40 is illustrated in greater detail in Figure 3B. The logic 40 includes finite state machine 46 and switching elements 47. The switching elements 47 are under the control of the finite state machine 46 and are used for forming an ATA communication channel between the host I/O port 18 and a selected one of the device I/O ports 20A-20C. *See* col. 9, lines 3-18. The logic 40 further includes combining elements 48. The combining elements 48 are used to combine separate interrupt and DMA request signals from ATA devices coupled to the device I/O ports 20A-20C into a single interrupt request signal INTRQ and a single DMA request signal DMARQ for the switch 14. *See* col. 9, lines 18-24.

In operation, the switch 14 operates in either a "connected" mode or a "disconnected" mode. These operating modes are illustrated in Figure 4. In the disconnected mode, logic 40 does not form a communication channel between host I/O port 18 and any device I/O port 20. When in the disconnected mode and switch 14 receives a "connect" command, switch 14 transitions from the disconnected mode to the connected mode. The connect command identifies a selected one of the device I/O ports 20. In the connected mode, logic 40 forms a communication channel between host I/O port 18 and the selected one of the device I/O ports 20. *See* col. 9, lines 28-36.

The communication channel formed between host I/O port 18 and the selected one of device I/O ports 20 in the connected mode conveys communications between host I/O port 18 and the selected one of device I/O ports 20. For example, the communication channel may provide a bi-directional path for communications according to the ATA standard between host I/O port 18 and the selected one of device I/O ports 20. In the connected mode, switch 14 conveys a communication received at the host I/O port 18 to the selected one of device I/O ports 20. Switch 14 also conveys a communication received at the selected one of device I/O ports 20

to host I/O port 18. As a result, in the connected mode, and except for the disconnect command, switch 14 is completely transparent to the controller coupled to host I/O port 18, and is transparent to the device coupled to the selected one of device I/O ports 20. *See* col. 9, lines 38-53.

When in the connected mode and switch 14 receives a "disconnect" command, switch 14 transitions from the connected mode to the disconnected mode. During a transition from the connected mode to the disconnected mode, logic 40 breaks the communication channel between host I/O port 18 and the selected one of the device I/O ports 20. *See* col. 9, lines 54-59.

Claims 1, 8, 13, and 24 are patentably distinct from the Talagala patent because the Talagala patent fails to disclose the combination of limitations recited by the respective claims.

For example, with respect to claim 1, the Talagala patent fails to disclose a memory module having a plurality of memory devices and a memory hub, the memory hub having a link interface for receiving memory requests for access to at least one of the memory devices, a memory device interface coupled to the memory devices, a switch for selectively coupling the link interface and the memory device interface, and a direct memory access (DMA) engine coupled through the switch to the memory device interface, the DMA engine generating memory requests for access to at least one of the memory devices to perform DMA operations.

As previously discussed, the Talagala patent is directed to a multi-I/O port ATA switch. The switch 14, which is illustrated in Figures 1-3, does not include a plurality of memory devices. The Examiner cites col. 8, lines 17-20 of the Talagala patent for disclosing a plurality of memory devices. However, the cited material describes the dual-switch embodiment shown in Figure 2 and that other ATA devices, in addition to device 30, can be coupled to the remaining I/O ports 20 of the switches 14A and 14B. The cited material does not describe including memory devices on either of the switches 14A or 14B, or that it would be desirable to do so. The switch 14 also does not include a memory hub having the elements as recited in claim 1. For example, the switch 14 does not have a DMA engine. The Examiner cites col. 9, lines 3-25 as disclosing a DMA engine of the memory hub as recited in claim 1. The material cited by the Examiner describes Figure 3B, which illustrates the host I/O port 18, the device I/O ports 20, and the logic 40 in detail for a particular embodiment of the switch 14. The only

mention of "DMA" in the material cited by the Examiner is with respect to the combining elements 48 that are included in the logic 40. As explained in the Talagala patent, the combining elements 48 receive separate interrupt and DMA request signals from the devices coupled to the device I/O ports 20A-20C and combine these separate signals into a single interrupt request signal (INTRQ) and a single DMA request signal (DMARQ) for the switch 14. The combining elements 48 is not a DMA controller, or a circuit that performs any functions similar to a DMA controller. The combining elements 48 merely take the plurality of interrupt and DMA request signals from devices coupled to the device I/O ports 20A-20C and generates one pair of interrupt and DMA request signals to be provided through the host I/O port 18.

Claims 8, 13, and 24 also recite limitations that the Talagala patent fails to disclose. With respect to claim 8, the Talagala patent fails to disclose a memory hub for a memory module having a plurality of memory devices that includes, among other things, a memory device interface for coupling to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices, and further includes a direct memory access (DMA) engine coupled through a switch to the memory device interface, the DMA engine generating memory requests for access to at least one of the memory devices to perform DMA operations. Claim 13 recites a memory system that includes a memory module similar to that recited in claim 1, and claim 24 recites a computer system that also includes a memory module similar to that recited in claim 1.

As previously discussed with respect to claim 1, the Talagala patent fails to disclose a memory module having a plurality of memory devices and a DMA engine coupled through a switch to a memory device interface and configured to generate memory requests for access to at least one of the memory devices to perform DMA operations. The Talagala patent is directed to a multi-device I/O port switch for establishing a communication channel one of several different ATA devices coupled to the device I/O ports. The switch described in Talagala patent includes the host I/O port 18, logic 40, and the device I/O ports 20. The switch does not include a memory hub, any memory devices, or a DMA engine. The switch is designed to allow a host device coupled to the host I/O port 18 communicate with one of several ATA devices coupled to the device I/O ports 20, which is in contrast to the conventional ATA controller that can connect to only two ATA devices.

For the foregoing reasons, claims 1, 8, 13, and 24 are patentably distinct from the Talagala patent. Claims 2 and 5, which depend from claim 1, claim 9, which depends from claim 8, claims 14, 15, 17, 18, and 21, which depend from claim 13, and claims 25, 26, 28, 29, and 32, which depend from claim 24, are similarly patentable based on their dependency from a respective allowable base claim. That is, each of the dependent claims further narrows the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. For the foregoing reasons, the rejection of claims 1, 2, 5, 8, 9, 13-15, 17, 18, 21, 24-26, 28, 29, and 32 under 35 U.S.C. 102(e) should be withdrawn.

As previously mentioned, claims 4, 6, 7, 11, 12, 20, 22, 23, 31, 33, and 34 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Talagala patent in view of the Jensen application, and claims 16 and 27 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Talagala patent in view of the Fredriksson application. The Jensen application has been cited by the Examiner as disclosing a cross-bar switch, synchronous dynamic random access memory devices, and DMA registers. *See* the Office Action, page 7. The Fredriksson application has been cited as disclosing a high-speed optical memory bus and an optical memory bus interface circuit for translating optical signals and electrical signals. *See* the Office Action, pages 7-8. Even if it is assumed for the sake of argument that the Examiner's characterizations of the Jensen and Fredriksson applications are accurate, they do not make up for the deficiencies of the Talagala patent as previously discussed with respect to claims 1, 8, 13, and 24. Consequently, the combined teachings of the Talagala patent and the Jensen application do not teach or suggest the combination of limitations of claims 4, 6, 7, 11, 12, 20, 22, 23, 31, 33, and 34, all of which are dependent from a respective allowable base claim. Additionally, the combined teachings of the Talagala patent and the Fredriksson application do not teach or suggest the combination of limitations recited by claims 16 and 27, which are also dependent from a respective allowable base claim. For the foregoing reasons, the rejection of claim 4, 6, 7, 11, 12, 20, 22, 23, 31, 33, and 34, and claims 16 and 27, under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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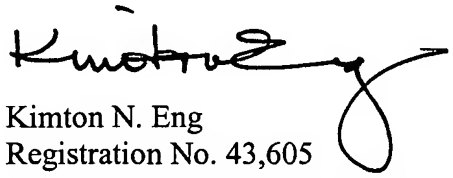

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